

ABSOLUTE MAXIMUM RATINGS (Voltage Reference)

| Rating | Symbol | Value |
|--|-------------------|------------------------|
| DC Supply Voltage | $V_{DD} - V_{SS}$ | -0.5 to 6 |
| Voltage, Any Pin to V_{SS} | V | -0.5 to $V_{DD} + 0.5$ |
| DC Current, Any Pin (Excluding V_{DD} , V_{SS}) | I | ± 10 |
| Operating Temperature | T_A | -40 to 85 |
| Storage Temperature | T_{stg} | -85 to 150 |

RECOMMENDED OPERATING CONDITIONS ($T_A = 0^\circ\text{C}$)

| Parameter | Symbol | Min | Max |
|---|-----------------------|-----|-----|
| DC Supply Voltage | V_{DD} | 4.5 | 5.5 |
| Power Dissipation ($\overline{P_D} = V_{DD}$) | $V_{DD} = 5\text{ V}$ | 100 | 100 |
| Power Dissipation ($\overline{P_D} = V_{SS}$) | $V_{DD} = 5\text{ V}$ | 100 | 100 |
| Frame Rate | M | 100 | 100 |
| CCI CLK Frequency (MSI = 8 kHz) UDLT-1 (CCI = 256 x MSI) UDLT-2 | C | 100 | 100 |
| Frame Rate Slip* | | | |
| Data Clock Rate (Master Mode) UDLT-1 UDLT-2 | TDC | 100 | 100 |
| SDCLK (UDLT-2 Only) | | | |
| Modulation Baud Rate UDLT-1 UDLT-2 | LO1, | 100 | 100 |

* The slave's crystal frequency divided by 512 (UDLT-1) or 1024 (UDLT-2) operation.

Product Preview

Universal Digital Loop Transceiver (UDLT-3)

Pin Selectable Master/Slave Limited Distance Modem

The MC145423 is a CMOS integrated circuit designed to integrate the major building blocks in digital subscriber voice/data telephone systems and remote data acquisition and control systems.

The UDLT-3 incorporates into one device, all the functions of the MC145421 (ISDN UDLT-2 master), MC145425 (ISDN UDLT-2 slave), MC145422 (UDLT-1 master), and MC145426 (UDLT-1 slave).

Since these modes/functions are pin selectable, the MC145423 can be used in telephone switch line cards, as well as remote data terminals or telsets or data terminals.

- $V_{DD} = 4.5\text{ V to }5.5\text{ V}$
- 28-Pin SOIC and TSSOP Packages
- Protocol Independent
- Pin Controlled Power-Down
- LI Sensitivity Control in Master Mode
- 2.048 MHz Output in Slave Mode

UDLT-2 Features

- Synchronous Full Duplex 160 kbps Voice and Data Communications in a 2B+2D Format for ISDN Companded Mode
- Provides CCITT Basic Access Data Transfer Rate (2B+2D) for ISDNs on a Single Twisted Pair Up to 1 km on 26 AWG Wire or Larger Cable

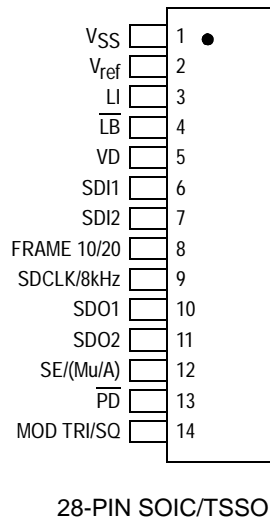
UDLT-1 Features

- Pin Controlled Loopback
- Automatic Power-Up/Down (Slave)
- Full Duplex Synchronous 64 kbps Voice/Data Channel and 8 kbps Signaling Data Channels Over One 26 AWG Wire or Larger Cable up to 2 km

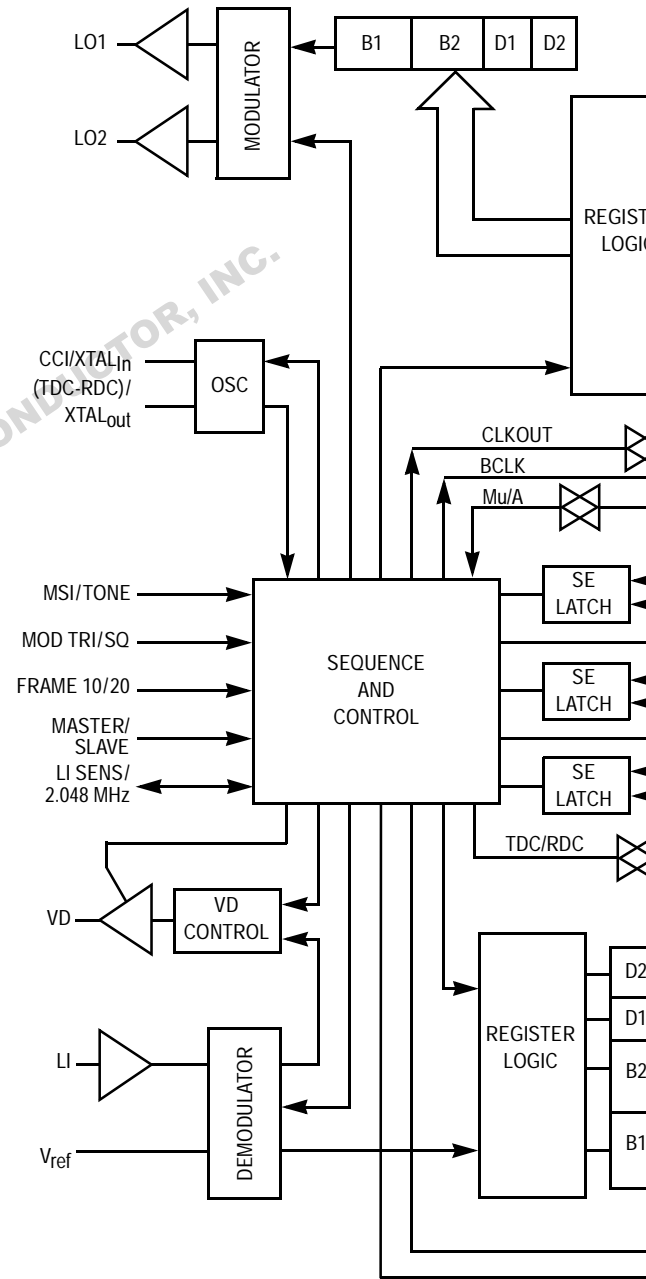
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PIN ASSIGN



BLOCK D



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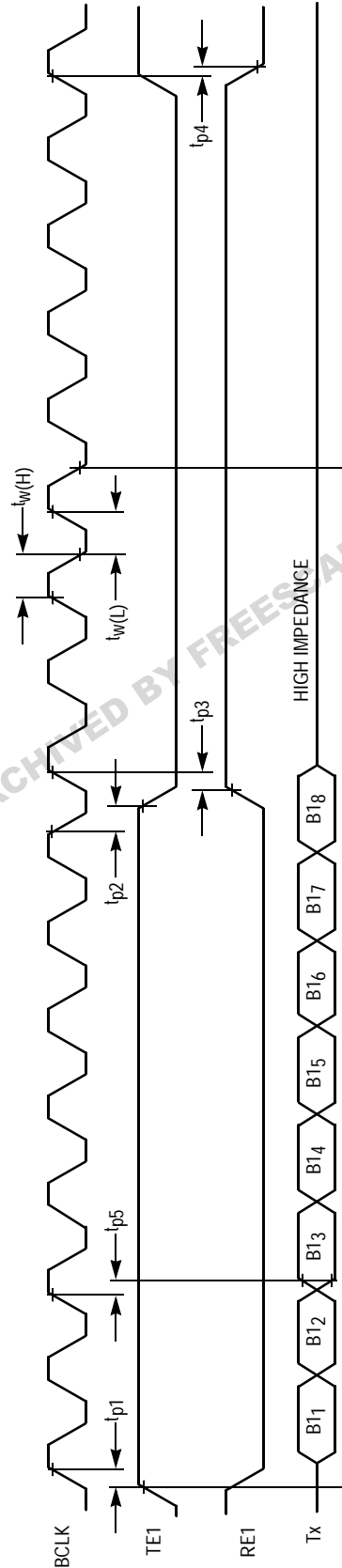


Figure 1. UDLT-1 Slave 1

DIGITAL CHARACTERISTICS ($V_{DD} = 5\text{ V} \pm 10\%$, $T_A =$

| Parameter |
|--|
| Input High Level |
| Input Low Level |
| Input Current (Digital Pins) |
| Input Current LI |
| Input Capacitance |
| Output High Current (Excluding Tx and $\overline{\text{PD}}$) |
| Output Current Low (Excluding Tx and $\overline{\text{PD}}$) |
| Tx Output High Current |
| Tx Output Low Current |
| $\overline{\text{PD}}$ Output High Current — Slave Mode* |
| $\overline{\text{PD}}$ Output Low Current — Slave Mode* |
| Tx, SDO1, SDO2, and VD Three-State Current |
| XTAL Output High Current |
| XTAL Output Low Current |

* To overdrive $\overline{\text{PD}}$ from a low level to 3.5 V, or a high level to 1.5 V req

ANALOG CHARACTERISTICS ($V_{DD} = 5\text{ V} \pm 10\%$, $T_A =$

| Parameter |
|--|
| Modulation Differential Amplitude ($R_L = 440\ \Omega$) |
| Modulation Differential Offset |
| V_{ref} Voltage, Typically $9/20 \times (V_{DD} - V_{SS})$ |
| PCM Tone Level |
| Demodulator Input Amplitude* |
| Demodulator Input Impedance (LI to V_{ref}) |

* The input level into the demodulator to reliably demodulate incoming

MASTER SWITCHING CHARACTERISTICS ($V_{DD} =$

| Parameter | Unit |
|---|------|
| Input Rise Time: All Digital Inputs | |
| Input Fall Time: All Digital Inputs | |
| Pulse Width: TDC, RDC, RE1, RE2, MSI, SDCLK (UDLT-2) | |
| CCI Duty Cycle | |
| Propagation Delay: MSI to SDO1, SDO2, VD ($\overline{PD} = V_{DD}$) TDC to Tx | |
| MSI, TE1, TE2, RE1, RE2 to TDC-RDC Setup Time | |
| TDC-RDC to MSI, TE1, TE2, RE1, RE2, Hold Time | |
| Rx to TDC-RDC Setup Time | |
| Rx to TDC-RDC Hold Time | |
| SDI1, SDI2 to MSI Setup Time | |
| SDI1, SDI2 to MSI Hold Time | |
| MSI Rising Edge to First SDCLK Falling Edge (UDLT-2 Only) | |
| TE Rising Edge to First Tx Data Bit Valid | |
| TDC-RDC Rising Edge to Tx Data Bits 2 – 8 Valid | |
| TE1, TE2 Falling Edge to Tx High Impedance | |
| SDCLK Rising Edge to SDO1, SDO2 Bit Valid (UDLT-2 Only) | |
| SDI1, SDI2 Data Setup (Data Valid Before SDCLK Falling Edge) (UDLT-2 Only) | |
| SDI1, SDI2 Data Hold (Data Valid After SDCLK Falling Edge) (UDLT-2 Only) | |
| \overline{PD} , \overline{LB} Setup (\overline{PD} , \overline{LB} Valid Before MSI Rising Edge) | |
| \overline{PD} , \overline{LB} Hold (\overline{PD} , \overline{LB} Valid After MSI Rising Edge) | |

SLAVE SWITCHING CHARACTERISTICS ($V_{DD} = 5$

| Parameter | Unit |
|--|------|
| Input Rise Time: All Digital Inputs | |
| Input Fall Time: All Digital Inputs | |
| Clock Output Pulse Width: BCLK | |
| Crystal Frequency | |
| Propagation Delay Times: EN1, EN2, TE1 Rising to BCLK (TONE = V_{DD}) EN1, EN2, TE1 Rising to BCLK (TONE = V_{SS}) BCLK to EN1, EN2, TE1 Falling RE1 Rising to BCLK (UDLT-1) RE1 Falling to BCLK (TONE = V_{DD}) (UDLT-1) RE1 Falling to BCLK (TONE = V_{SS}) (UDLT-1) BCLK to Tx TE1, TE2 to SDO1, SDO2 | |
| Rx to BCLK Setup Time | |
| Rx to BCLK Hold Time | |
| SDI1, SDI2 to TE Setup Time | |
| SDI1, SDI2 to TE Hold Time | |
| EN1, EN2 Rising Edge to DCLK Rising Edge (UDLT-2) | |
| EN1, EN2 Rising Edge to First Tx Data Bit Valid | |
| BCLK Rising Edge to Tx Data Bits 2 – 8 Valid | |
| DCLK Pulse Width High (UDLT-2) | |
| DCLK Pulse Width Low (UDLT-2) | |
| DCLK Rising Edge to SDO1, SDO2 (UDLT-2) | |
| SDI1, SDI2 Setup (SDI1, SDI2 Valid Before DCLK Falling Edge) (UDLT-2) | |
| SDI1, SDI2 Hold (SDI1, SDI2 Valid After DCLK Falling Edge) (UDLT-2) | |
| EN1, TE1 Rising Edge to VD Valid | |

SE PIN TIMING

| Parameter | Unit |
|---|------|
| \overline{LB} , \overline{PD} Hold (\overline{LB} , \overline{PD} Valid After SE Falling Edge) | |
| SDO1, SDO2, VD High Impedance After SE Falling Edge | |
| SDO1, SDO2, VD Valid After SE Rising Edge | |
| \overline{LB} , \overline{PD} Setup (\overline{LB} , \overline{PD} Valid Before SE Rising Edge) | |

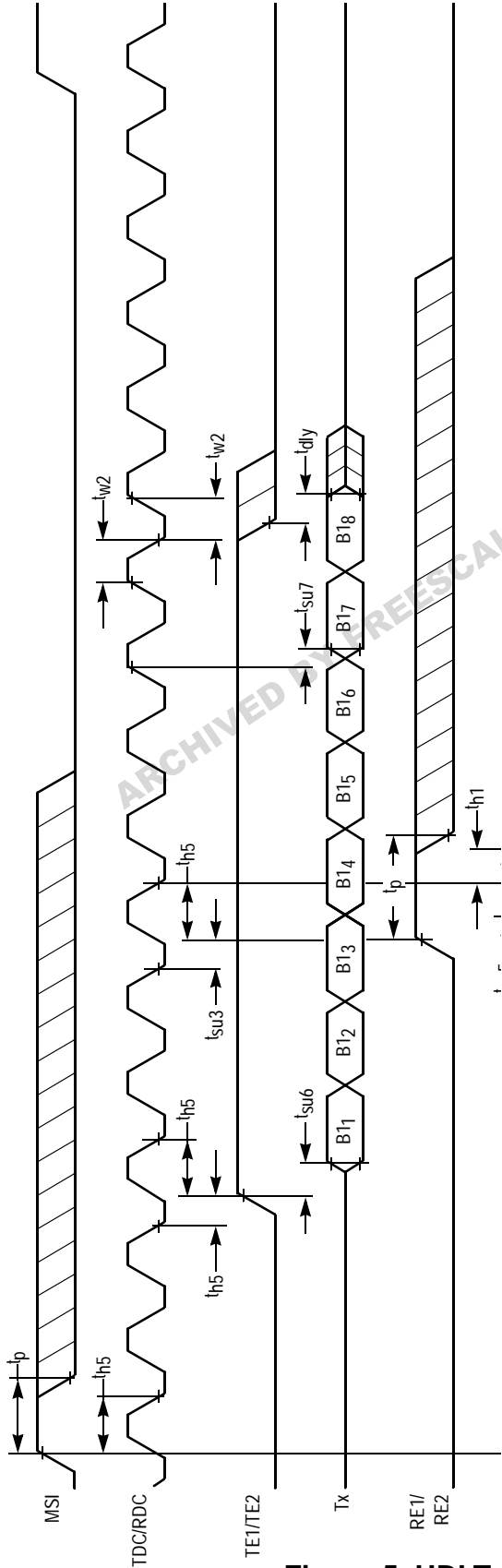


Figure 5. UDLT-

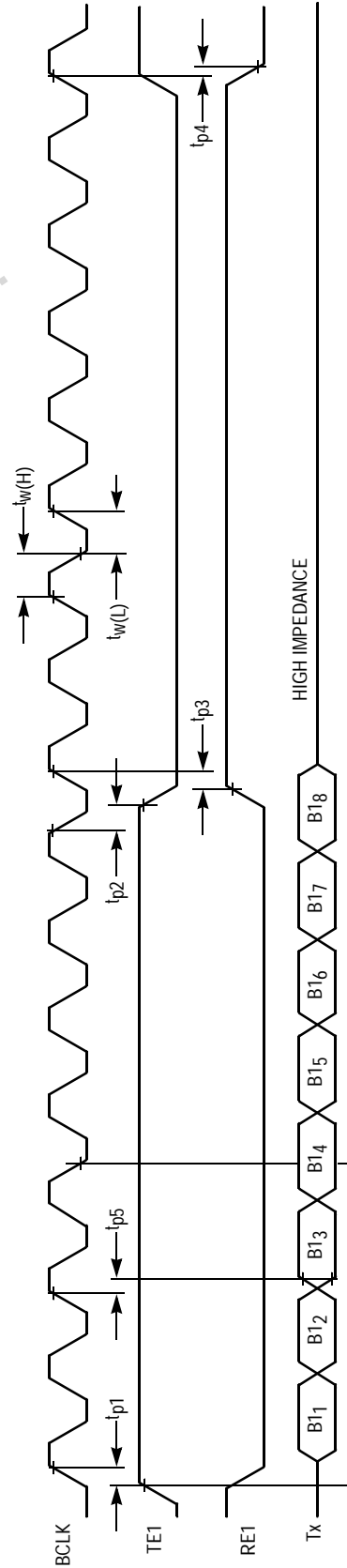


Figure 2. UDLT-1 Slave

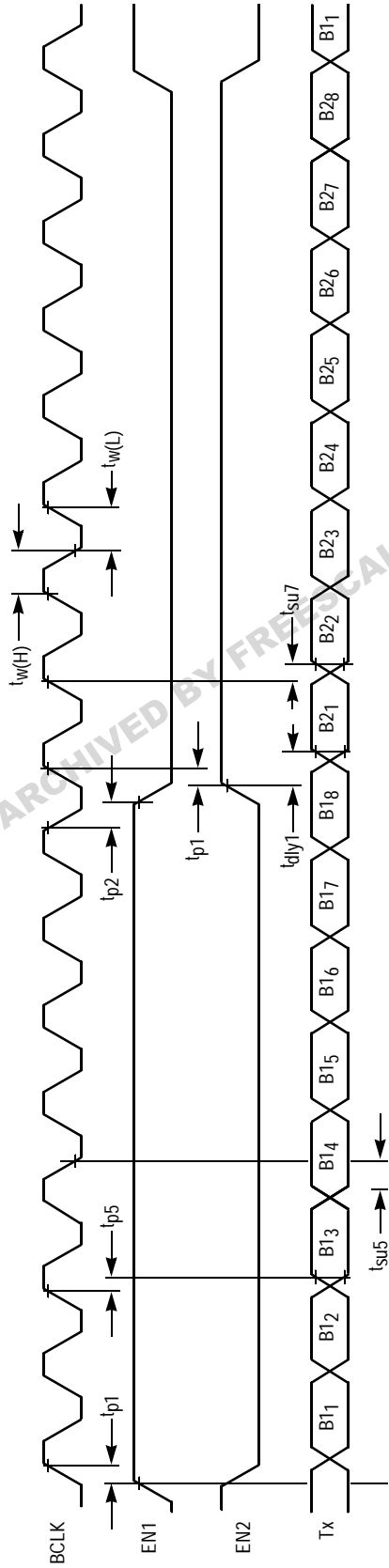


Figure 3. UDLT-

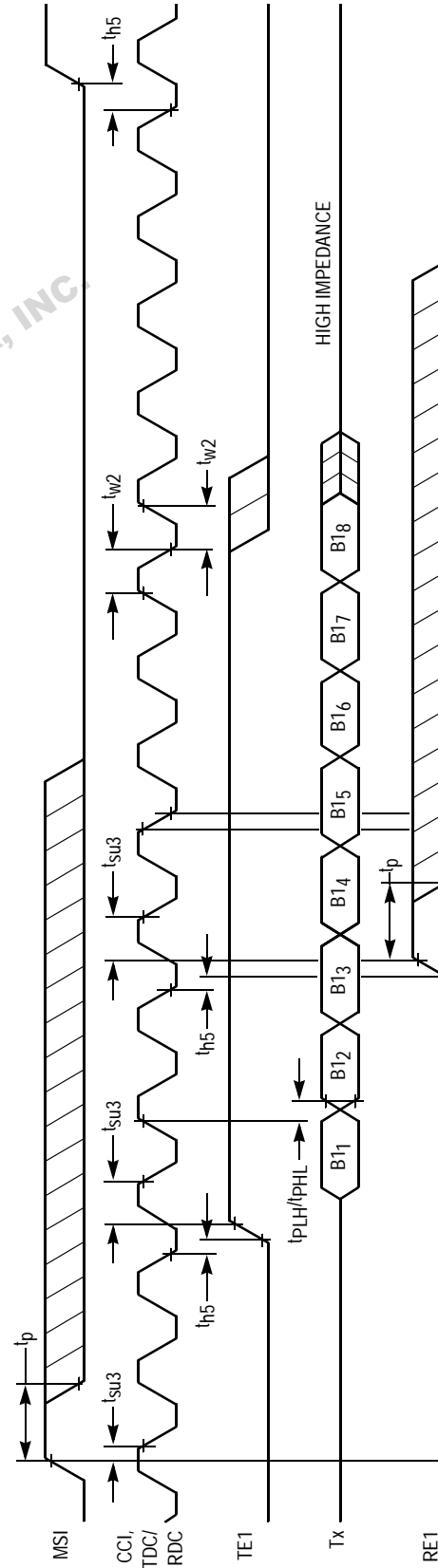


Figure 4. UDLT-

MC145423 UDLT-3 PIN STATES FOR UDLT-1 SLA

| MC145423 | | | UDLT-1 Slave Mode Powered-Up | |
|----------|------------------|--------|------------------------------|----------------------------|
| Pin No. | Pin Name | In/out | Normal | $\overline{\text{LB}}$ Low |
| 23 | RE2/ BCLK | Output | BCLK = 128 kHz | BCLK = 0 |
| 24 | Rx | Input | 64 kbps Data In | Don't Care |
| 25 | LO2 | Output | Modulator Out | Modulator Out |
| 26 | LO1 | Output | Modulator Out | Modulator Out |
| 27 | MASTER/ SLAVE | Input | 1 | 1 |
| 28 | V _{DD} | Power | +V | +V |

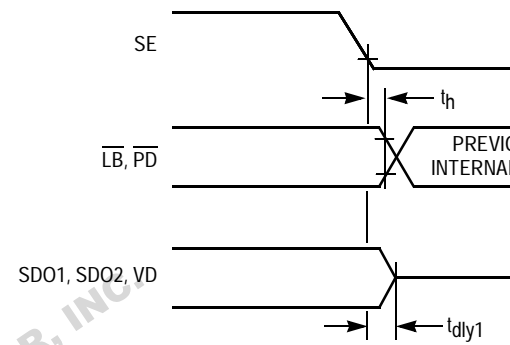


Figure 6. SE

MC145423 UDLT-3 PIN STATES FOR UDLT-1 MAS

| MC145423 | | | UDLT-1 Master Mode Powered-Up | |
|----------|------------------------|---------------|-------------------------------|----------------------------|
| Pin No. | Pin Name | In/out | Normal | $\overline{\text{LB}}$ Low |
| 1 | V _{SS} | Power | Power Supply Gnd | Power Gnd |
| 2 | V _{ref} | Analog Ref | AGND V _{DD} /2 | AGND |
| 3 | LI | Input | Analog In | Don't Care |
| 4 | $\overline{\text{LB}}$ | Input | 1 | 0 |
| 5 | VD | Output | Digital out | Digital out |
| 6 | SDI1 | Input | 8 kbps Data In | 8 kbps Data In |
| 7 | SDI2 | Input | 8 kbps Data In | 8 kbps Data In |
| 8 | FRAME 10/20 | Input | 0 | 0 |
| 9 | SDCLK | Don't Care | High Impedance | High Imp edance |
| 10 | SDO1 | Output | 8 kbps Data Out | 8 kbps Data Out |
| 11 | SDO2 | Output | 8 kbps Data Out | 8 kbps Data Out |
| 12 | SE/(Mu/A) | Input | 1 | 1 |
| 13 | $\overline{\text{PD}}$ | Input | 1 | 1 |
| 14 | MOD TRI/SQ | Input | 0 | 0 |
| 15 | Tx | Output | 64 kbps Data Out | 64 k Data Out |
| 16 | EN2-TE2/ SIE/B1B2 | Input | SIE Digital In | SIE Di gital In |

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SOIC PACKAGE PIN

UDLT-3 PINOUT VERSUS MC145421DW/22DW/25 (UDLT-1/UDLT-2 MASTER/SLAVE) PINOUT

| UDLT-3 MC145423 | | UDLT-1 Master MC145422 | | UDLT-1 MC145421 | |
|-----------------|-----------------------------|------------------------|----------|-----------------|----------|
| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
| 1 | VSS | 1 | VSS | 1 | |
| 2 | Vref | 2 | Vref | 2 | |
| 3 | LI | 3 | LI | 3 | |
| 4 | LB | 5 | LB | 5 | |
| 5 | VD | 6 | VD | 6 | |
| 6 | SDI1 | 7 | SI1 | 7 | |
| 7 | SDI2 | 9 | SI2 | 9 | |
| 8 | FRAME 10/20 | Logic 0 | | Log | |
| 9 | SDCLK/8kHz | High Impedance | | SDC | |
| 10 | SDO1 | 8 | SO1 | 8 | |
| 11 | SDO2 | 10 | SO2 | 10 | |
| 12 | SE/(Mu/A) | 11 | SE | 11 | |
| 13 | PD | 12 | PD | 12 | |
| 14 | MOD TRI/SQ | Logic 0 | | Log | |
| 15 | Tx | 16 | Tx | 15 | |
| 16 | EN2-TE2/SIE/B1B2 | 14 | SIE | B1 Log | |
| 17 | EN1-TE1 | 15 | TE1 | 14 | |
| 18 | MSI/TONE | 13 | MSI | 13 | (|
| 19 | CCI/XTAL _{in} | 17 | CCI | 16 | (X |
| 20 | TDC-RDC/XTAL _{out} | 18 | TDC/RDC | 17 | (XT |
| 21 | LI SENS/2.048 MHz | Logic 0 LI SENS | | 2.048 M | |
| 22 | RE1/CLKOUT | 20 | RE1 | 20 | |
| 23 | RE2/BCLK | High Impedance | | 18 | (B |
| 24 | Rx | 19 | Rx | 19 | |
| 25 | LO2 | 22 | LO2 | 22 | |
| 26 | LO1 | 23 | LO1 | 23 | |
| 27 | MASTER/SLAVE | Logic 0 | | Log | |
| 28 | VDD | 24 | VDD | 24 | |

MC145423 UDLT-3 PIN STATES FOR UDLT-1 SLAVE

| MC145423 | | | UDLT-1 Slave Mode Powered-Up | |
|----------|-----------------------------|------------|-------------------------------|-------------------------------|
| Pin No. | Pin Name | In/out | Normal | LB Low |
| 1 | VSS | Power | Power Supply Gnd | Power Supply Gnd |
| 2 | Vref | Analog Ref | AGND VDD/2 | AGND VDD/2 |
| 3 | LI | Input | Analog In | Analog In |
| 4 | LB | Input | 1 | 0 |
| 5 | VD | Output | Digital Out | Digital Out |
| 6 | SDI1 | Input | 8 kbps Data In | 8 kbps Data In |
| 7 | SDI2 | Input | 8 kbps Data In | 8 kbps Data In |
| 8 | FRAME 10/20 | Input | 0 | 0 |
| 9 | SDCLK/8kHz | Output | SDCLK/8kHz | SDCLK/8kHz |
| 10 | SDO1 | Output | 8 kbps Data Out | 8 kbps Data Out |
| 11 | SDO2 | Output | 8 kbps Data Out | 8 kbps Data Out |
| 12 | SE/(Mu/A) | Input | 1= Mu, 0 = A | 1= Mu, 0 = A |
| 13 | PD | I/O | 1 | 1 |
| 14 | MOD TRI/SQ | Input | 0 | 0 |
| 15 | Tx | Output | 64 kbps Data Out | 64 kbps Data Out |
| 16 | EN2-TE2/SIE/B1B2 | Input | 1/0 B1B2 | 1/0 B1B2 |
| 17 | EN1-TE1 | Output | EN1 = 8 kHz | EN1 = 8 kHz |
| 18 | MSI/TONE | Input | 1/0 TONE | 1/0 TONE |
| 19 | CCI/XTAL _{in} | Input | XTAL _{in} 4.096 MHz | XTAL _{in} 4.096 MHz |
| 20 | TDC-RDC/XTAL _{out} | Output | XTAL _{out} 4.096 MHz | XTAL _{out} 4.096 MHz |
| 21 | LI SENS/2.048 MHz | Output | 2.048 MHz | 2.048 MHz |
| 22 | RE1/CLKOUT | Output | RE1 = 8 kHz | RE1 = 8 kHz |

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PIN DESCRIPTIONS

V_{SS}
Negative Supply (Pin 1)

This is the most negative power pin, and should be tied to system ground (0 V).

V_{ref}
Voltage Reference Output (Pin 2)

This is the output from the internal reference supply (mid-supply) and should be bypassed to both V_{SS} and V_{DD} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external load should be placed on this pin.

LI
Line Input (Pin 3)

This pin is the input to the demodulator for the incoming bursts. This input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LB
Loopback Low Input (Pin 4)

Master Mode: A low on this pin ties the internal modulator output to the internal demodulator input, which loops the entire burst for testing purposes. During the loopback operation, the LI input is ignored, and the LO1 and LO2 outputs are driven to equal voltages. The state of the LB pin is internally latched if the SE pin is held low. This feature is only active when the PD input is high.

Slave Mode: When this pin is low and PD is high, the incoming B channels from the master are burst back to the master, instead of the Rx B channel input data. The SDI1 and SDI2 functions operate normally in this mode, and the BCLK (pin 23) is held low. Additionally, for both the UDLT-1 and UDLT-2 mode, when the TONE (pin 18) and loopback functions are active simultaneously, the loopback function overrides the TONE function.

VD
Valid Data Output (Pin 5)

A high level on this pin indicates that a valid line transmission has been demodulated. A valid line transmission burst is determined by proper

MC145423 UDLT-3 PIN STATES FOR UDLT-1 MASTER MODE

| MC145423 | | | UDLT-1 Master Mode Powered-Up | |
|----------|---------------------------------|------------|----------------------------------|---------------------------|
| Pin No. | Pin Name | In/out | Normal | LB Low |
| 17 | EN1-TE1 | Input | TE1 8 kHz | TE1 8 kHz |
| 18 | MSI/TONE | Input | MSI 8 kHz | MSI 8 kHz |
| 19 | CCI/ XTAL _{in} | Input | CCI 2.048 MHz | CCI 2.048 MHz |
| 20 | TDC-RDC/ XTAL _{out} | Input | TDC-RDC Data Clk | TDC-RDC Data Clk |
| 21 | LI SENS/ 2.048 MHz | Input | Digital In LI Sensitivity | Digital In LI Sensitivity |
| 22 | RE1/ CLKOUT | Input | RE1 8 kHz | RE1 8 kHz |
| 23 | RE2/ BCLK | Don't Care | High Impedance | High Impedance |
| 24 | Rx | Input | 64 kbps Data In | 64 kbps Data In |
| 25 | LO2 | Output | Modulator Out | LO2 = |
| 26 | LO1 | Output | Modulator Out | LO1 = |
| 27 | MASTER/ SLAVE | Input | 0 | 0 |
| 28 | V _{DD} | Power | +V | + |

MC145423 UDLT-3 PIN STATES FOR UDLT-2 SLAVE MODE

| MC145423 | | | UDLT-2 Slave Mode Powered-Up | |
|----------|------------------|------------|---------------------------------|-------------------------|
| Pin No. | Pin Name | In/out | Normal | LB Low |
| 1 | V _{SS} | Power | Power Supply Gnd | Power Supply Gnd |
| 2 | V _{ref} | Analog Ref | AGND V _{DD} /2 | AGND V _{DD} /2 |
| 3 | LI | Input | Analog In | Analog In |
| 4 | LB | Input | 1 | 0 |
| 5 | VD | Output | Digital Out | Digital Out |
| 6 | SDI1 | Input | 16 kbps Data In | 16 kbps Data In |
| 7 | SDI2 | Input | 16 kbps Data In | 16 kbps Data In |
| 8 | FRAME 10/20 | Input | 1 | 1 |
| 9 | SDCLK | Output | 16 kHz | 16 kHz |

MC145423 UDLT-3 PIN STATES FOR UDLT-2 SLA

| MC145423 | | | UDLT-2 Slave Mode Powered-Up | |
|----------|------------------------------|--------|------------------------------|----------------------------|
| Pin No. | Pin Name | In/out | Normal | $\overline{\text{LB}}$ Low |
| 10 | SDO1 | Output | 16 kbps Data Out | 16 kbps Data Out |
| 11 | SDO2 | Output | 16 kbps Data Out | 16 kbps Data Out |
| 12 | SE/ (Mu/A) | Input | 1/0 Mu/A | 1/0 Mu/A |
| 13 | $\overline{\text{PD}}$ | I/O | 1 | 1 |
| 14 | MOD TRI/SQ | Input | 1 | 1 |
| 15 | Tx | Output | 128 kbps Data Out* | 128 kbps Data Out* |
| 16 | EN2-TE2/ SIE/B1B2 | Output | EN2 8 kHz | EN2 8 kHz |
| 17 | EN1-TE1 | Output | EN1 8 kHz | EN1 8 kHz |
| 18 | MSI/ TONE | Input | 1/0 Tone | 1/0 Tone |
| 19 | CCI/ XTAL _{in} | Input | XTAL 8.192 MHz | XTAL 8.192 MHz |
| 20 | TDC-RDC/ XTAL _{out} | Output | XTAL 8.192 MHz | XTAL 8.192 MHz |
| 21 | LI SENS/ 2.048 MHz | Output | 2.048 MHz | 2.048 MHz |
| 22 | RE1/ CLKOUT | Output | RE1 8 kHz | RE1 8 kHz |
| 23 | RE2/ BCLK | Output | BCLK 128 kHz | BCLK = 0 |
| 24 | Rx | Input | 128 kbps Data In | Don't Care |
| 25 | LO2 | Output | Modulator Out | Modulator Out |
| 26 | LO1 | Output | Modulator Out | Modulator Out |
| 27 | MASTER/ SLAVE | Input | 1 | 1 |
| 28 | V _{DD} | Power | +V | +V |

* Tx is high impedance when TE1 and TE2 are both low, simultaneous
Tx is undefined when TE1 and TE2 are both high, simultaneously.

MC145423 UDLT-3 PIN STATES FOR UDLT-2 MAS

| MC145423 | | | UDLT-2 Master | |
|----------|------------------------------|------------|-------------------------|----------------------------|
| Pin No. | Pin Name | In/out | Normal | $\overline{\text{LB}}$ Low |
| 1 | V _{SS} | Power | Power Supply Gnd | Power Supply Gnd |
| 2 | V _{ref} | Analog Ref | AGND V _{DD} /2 | AGND |
| 3 | LI | Input | Analog In | Don't Care |
| 4 | $\overline{\text{LB}}$ | Input | 1 | 0 |
| 5 | VD | Output | Digital Out | Digital Out |
| 6 | SDI1 | Input | 16 kbps Data In | 16 kbps Data In |
| 7 | SDI2 | Input | 16 kbps Data In | 16 kbps Data In |
| 8 | FRAME 10/ 20 | Input | 1 | 1 |
| 9 | SDCLK | Input | 16 kHz | 16 kHz |
| 10 | SDO1 | Output | 16 kbps Data Out | 16 kbps Data Out |
| 11 | SDO2 | Output | 16 kbps Data Out | 16 kbps Data Out |
| 12 | SE/(Mu/A) | Input | 1 | 1 |
| 13 | $\overline{\text{PD}}$ | Input | 1 | 1 |
| 14 | MOD TRI/SQ | Input | 1 | 1 |
| 15 | Tx | Output | 128 kbps* Data Out | 128 kbps* Data Out |
| 16 | EN2-TE2/ SIE/B1B2 | Input | TE2 8 kHz | TE2 8 kHz |
| 17 | EN1-TE1 | Input | TE1 8 kHz | TE1 8 kHz |
| 18 | MSI/TONE | Input | 8 kHz | 8 kHz |
| 19 | CCI/XTAL _{in} | Input | CCI 4.096 MHz | CCI 4.096 MHz |
| 20 | TDC-RDC/ XTAL _{out} | Input | TDC-RDC Data Clk | TDC-RDC Data Clk |
| 21 | LI SENS/ 2.048 MHz | Input | Digital In Sensitivity | Digital In Sensitivity |
| 22 | RE1/ CLKOUT | Input | RE1 8 kHz | RE1 8 kHz |
| 23 | RE2/BCLK | Input | RE2 8 kHz | RE2 8 kHz |
| 24 | Rx | Input | 128 kbps Data In | 128 kbps Data In |
| 25 | LO2 | Output | Modulator Out | LO2 = 0 |
| 26 | LO1 | Output | Modulator Out | LO1 = 0 |
| 27 | MASTER/ SLAVE | Input | 0 | 0 |
| 28 | V _{DD} | Power | +V | +V |

* Tx is high impedance when TE1 and TE2 are both low, simultaneous
Tx is undefined when TE1 and TE2 are both high, simultaneously.

data buffer with data from the Rx pin on the next eight falling edges of the TDC-RDC clock. The RE1 and RE2 enables should be roughly leading edge aligned with the TDC-RDC data clock. These enables are rising edge sensitive and need not be high for the entire B channel input period.

Slave Mode (CLKOUT UDLT-2): This pin serves as a buffered output of the crystal frequency divided by two.

RE2/BCLK

Receive Data Enable Input 2 or B Channel Data Clock Output (Pin 23)

Master Mode (UDLT-1): This pin is high impedance.

Master Mode (RE2 UDLT-2): See pin description for RE1 (pin 22).

Slave Mode (BCLK UDLT-1 and UDLT-2):

This output provides the data clock for the telset codec-filter. This clock signal is 128 kHz and begins operating upon the successful demodulation of a burst from the master. At this time, EN1-TE1 goes high and BCLK starts toggling. BCLK remains active for 16 periods, at the end of which time it remains low until another burst is received from the master. In this manner, synchronization between the master and slave is established and any clock slippage is absorbed each frame. If TONE (pin 18) is brought high, then EN1-TE1/RE1 are generated from an internal oscillator until TONE is brought low, or an incoming burst from the master is received. BCLK is disabled when \overline{LB} is held low.

Rx

Receive Data Input (Pin 24)

Master Mode (UDLT-1): The 8-bit B channel data is clocked into the device on this pin, on the falling edges of TDC-RDC, under the control of RE1.

Slave Mode (UDLT-1): The 8-bit B channel data from the telset PCM codec-filter is input on this pin on the eight falling edges of BCLK after RE1 goes high, when EN2-TE2/SIE/B1B2, pin 16 is low. When EN2-TE2/SIE/B1B2, pin 16 is high, the receive data word is latched in during the high period of EN1-TE1, pin 17

FRAME 10/20 (Pin 8)

The UDLT series of transceivers are designed to operate using a ping-pong transmission scheme with an 8 kHz burst rate. Each frame the master device “pings” a burst of data to the slave, which responds with a “pong” burst of data. This pin selects whether this 8 kHz frame will have a 10-bit data burst for UDLT-1 compatibility or a 20-bit data burst for UDLT-2 compatibility.

A logic low (0 V) selects the UDLT-1 (MC145422/MC145426) mode. This sets the device to operate with one 64 kbps voice/data channel and two 8 kbps signaling channels. A logic high (V_{DD}) on this pin selects the UDLT-2 (MC145421/MC145425) mode. This sets the device to operate with two 64 kbps channels and two 16 kbps channels (2B+2D).

SDCLK

D Channel Signaling Data Clock Input (Pin 9)

Master Mode (UDLT-2): This is the transmit and receive data clock input for both D channels. See SDO1 and SDO2 pin descriptions for more information.

Master Mode (UDLT-1): High impedance.

Slave Mode (UDLT-2): This is the transmit and receive data clock output for both D channels. It starts on demodulation of a burst from the master device. This signal is rising-edge aligned with the EN1 and BCLK signals. After the demodulation of a burst, the SDCLK line completes two cycles and then remains low until the next burst from the master is demodulated. In this manner, synchronization with the master is established and any clock slip between master and slave is absorbed each frame.

Slave Mode (UDLT-1): This pin outputs 8 kHz equivalent to TE1.

SDO1 and SDO2

D Channel Signaling Data Outputs 1 and 2 (Pins 10 and 11)

Master Mode (UDLT-2): These serial outputs provide the 16 kbps D channel signaling information from the incoming burst. Two data bits should be clocked out of each of these two outputs between the rising edges of the MSI frame reference clock. The rising edge of MSI produces the first bit of each D channel on its respective pin. Circuitry then searches for a negative D channel clock edge. This

250 μ s have elapsed without a burst from the master being successfully demodulated. This allows the slave device to self power-up and power-down in demand powered loop systems. When held low, the device powers down and the only active circuitry, is that which is necessary for the demodulation of data. When held high, the device is powered up and transmits normally in response to received bursts from the master.

MOD TRI/SQ Modulation Select (Pin 14)

A logic low (0 V) on this pin selects the MDPSK modulation which has a slew controlled voltage output for reduced EMI/RFI. This output looks like a triangle waveform that is modulated with different angles for the peaks. A logic high (V_{DD}) on this pin, selects square wave output for maximum power to the line.

Tx Transmit Data Output (Pin 15)

Master Mode (UDLT-1): This pin is high impedance when TE1 is low. When TE1 is high, this pin presents new 8-bit B channel data on rising edges of TDC-RDC.

Slave Mode (UDLT-1): B channel data is output on this pin on the rising edge of BCLK, while TE1 is high. This pin is high impedance when TE1 is low.

Master Mode (UDLT-2): This pin is high impedance when both TE1 and TE2 are low. This pin serves as an output for B channel information received from the slave device. The B channel data is under control of TE1 and TE2 and TDC-RDC.

Slave Mode (UDLT-2): This pin is an output for the B channel data received from the master. B channel 1 data is output on the first eight cycles of the BCLK output when EN1 is high. B channel 2 data is output on the next eight cycles of the BCLK, when EN2 is high. B channel data bits are clocked out on the rising edge of the BCLK output pin.

EN2-TE2/SIE/B1B2 B Channel 2 Enable Output or Signal Insert Enable (Pin 16)

Master Mode (SIE UDLT-1): In this mode, this pin functions as SIE. When held high, this pin causes signal bit 2, as received from the slave, to be inserted into the LSB of the outgoing PCM word at the Tx pin. The SDI2 pin will be ignored, and in its place, the LSB

pin is also updated on the rising edge of the EN1 signal.

MSI/TONE Master Sync Input or Tone Enable Input (Pin 18)

Master Mode (MSI): This pin is the master 8 kHz frame reference input. The rising edge of MSI loads B and D channel data, which had been input during the previous frame, into the modulator section of the device, and initiates the outbound burst onto the twisted pair cable. The rising edge of MSI also initiates the buffering of the B and D channel data demodulated during the previous frame. MSI should be approximately leading edge aligned with the TDC-RDC data clock input signal.

Slave Mode (TONE): A high on this pin causes a 500 Hz square wave PCM tone to be inserted in place of the demodulated data. This feature allows the designer to provide audio feedback for telset keyboard depressions.

CCI/XTAL_{in} Convert Clock Input or Crystal Input (Pin 19)

Master Mode (CCI UDLT-1): A 2.048 MHz clock signal should be applied to this pin. This signal is used for internal sequencing and control. This signal should be frequency and phase coherent with MSI for optimum performance.

Slave Mode (XTAL_{in} UDLT-1): A 4.096 MHz crystal is tied between this pin and XTAL_{out} (pin 20). A 10 M Ω resistor across this pin and XTAL_{out} and 25 pF capacitors from this pin and XTAL_{out} to V_{SS} are required for stability and to ensure start-up. This pin may be driven from an external source. XTAL_{out} should be left open if an external signal is used on this input.

Master Mode (CCI UDLT-2): An 8.192 MHz clock should be supplied to this input. The 8.192 MHz input should be 50% duty cycle. This signal may free run with respect to all other clocks without performance degradation.

Slave Mode (XTAL_{in} UDLT-2): Normally, an 8.192 MHz crystal is tied between this pin and the XTAL_{out} (pin 20). A 10 M Ω resistor between XTAL_{in} and XTAL_{out} and 25 pF capacitors from XTAL_{in} and XTAL_{out} to V_{SS} are required to ensure stability and start-up. XTAL_{in} may also be driven with an external 8.192 MHz signal if a crystal is not

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